

A high-voltage amplifier for traveling-wave Stark deceleration F SCI

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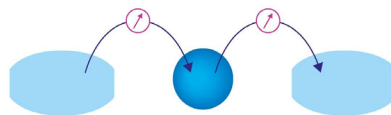
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A high-voltage amplifier for traveling-wave Stark deceleration

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Controlling high voltage is a critical aspect of Stark deceleration, a technique that uses electric fields to produce slow molecules. Traditionally, Stark deceleration required only commercial high-voltage switches to operate. However, a new continuous version of Stark deceleration, which promises significantly improved performance, requires chirped sinusoidal voltages. The complexity of the electronics needed to run this new decelerator has restricted the implementation for all but a few groups. The challenge is to create high-voltage amplifiers that have a frequency range of tens of kilohertz down to DC and that can source and sink enough current (~ 1 A) to drive the capacitive load of the decelerator. We present a new high-voltage linear amplifier for driving in-vacuum electrodes for traveling-wave Stark deceleration. The amplifier has a gain of 12 000, output voltages up to ± 10 kV, instantaneous currents up to 1.5 A, and a frequency range from 30 kHz down to DC. This makes the amplifier suitable for traveling-wave Stark deceleration of a supersonic molecular beam down to rest. *Published by AIP Publishing.* <https://doi.org/10.1063/1.5040267>

I. INTRODUCTION

Stark deceleration is a molecular manipulation technique that uses time-varying inhomogeneous electric fields to produce packets of slow, cold molecules.¹ In this technique, large electric-field gradients are created inside a vacuum chamber via application of large potential differences between electrodes. These gradients exert Stark-effect forces on polar molecules in particular quantum states. With the correct electrode geometry and temporal control of the applied potentials, molecular beams can be decelerated. The resulting beam velocity can be tuned from several hundred m/s down to rest. These beams can then be loaded into static electric or magnetic traps for collision studies^{2–5} or used in low velocity experiments.^{6–8}

There are two main approaches to Stark deceleration, which use distinct electrode geometries and applied voltage waveforms. The first approach, pulsed-pin Stark deceleration (PPSD), uses crossed-pin electrodes and discrete digital voltages to decelerate a pulsed molecular beam. While PPSD is relatively easy to implement using commercially available high-voltage switches to control the potentials on the electrodes, there are well-documented loss mechanisms^{9,10} that reduce the efficiency of the deceleration process, particularly at low beam velocities. The second approach, traveling-wave Stark deceleration (TWSD), uses ring electrodes and sinusoidal analog voltages to create a continuously moving Stark potential well.^{11,12} Because the molecules are always confined while being decelerated, TWSD is able to avoid many of the instabilities and inefficiencies⁹ inherent in PPSD.^{1,13} Additionally, by chirping the frequency of the analog voltages down to DC, the traveling potential well comes to a standstill and can serve as a trap.¹⁴ Thus, TWSD also offers the option of

efficiently trapping decelerated molecules, resulting in greater trapped molecule densities than in previous Stark decelerator geometries.

The challenge to implementing TWSD is creating the high-voltage driving electronics. The traditional approach for creating high voltage waveforms, using transformers, fails at low frequencies and only has a narrow tuning range. Thus, linear amplifiers must be used to drive the traveling-wave decelerator. The necessary bandwidth, voltage, current, and heat dissipation characteristics of an amplifier are set by the particular geometry of the decelerator. Our decelerator is of similar design to previously constructed ring Stark decelerators^{11,15} and has 624 tantalum ring electrodes with every eighth ring electrically connected. Therefore, TWSD requires eight analog amplifiers in order to produce the chirped frequency sine-wave voltages. The rings are made of 0.04 in. diameter wire with an inner diameter of 0.16 in. The center-to-center spacing between rings is 0.08 in. This decelerator is designed to serve a similar role to our pulsed-pin Stark decelerator¹⁶ and will be used with the same high-voltage power supplies, pulsed valve, and state-selective detection system used previously.¹⁷

In TWSD, the Stark potential well must have an initial longitudinal speed that corresponds to the initial speed of the molecular beam. The speed of the potential well must then be reduced to the desired final speed of the molecular packet. Using the initial and final speeds of the molecular packet and the length of one Stark potential well, we can calculate the required bandwidth of the amplifier. The longitudinal length of one Stark potential well is determined by l , the electrode spacing, and p , the ring periodicity (i.e., the number of rings that create a single period of the sine wave). To produce a potential well with a longitudinal velocity v , the frequency of the output voltage waveform is

$$f = \frac{v}{pl}. \quad (1)$$

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For most traveling-wave Stark decelerators constructed to date^{11,14,18,19} l is 1.5 mm, while for our decelerator l is 0.04 in. (2.032 mm). All traveling-wave decelerators built to date have a p of 8. For a supersonic molecular beam seeded in krypton, the initial velocity is between 400 and 450 m/s, setting the upper end of the bandwidth to 28 kHz. If the molecules are to be trapped after deceleration, the final velocity must be zero. Therefore, the high-voltage amplifier must have a bandwidth of at least 28 kHz down to DC. The amplifier presented here is designed to run from 30 kHz down to DC in order to provide flexibility with the output waveform. This bandwidth, on its own, is not extremely challenging to achieve, but there are also demanding voltage and current specifications to be met.

The peak output voltage of the amplifier and geometry of the decelerator set the depth of the Stark potential well, which in turn sets the limit on the magnitude of deceleration. The larger the amplitude of the voltage and the closer the rings are spaced, the greater the electric fields and depth of the potential well produced. The maximum achievable voltage on a Stark decelerator electrode is determined by either the high-voltage power supplies or the maximum voltage difference that can be supported between two adjacent electrodes. While a 1 mm gap can support up to 20 kV,²⁰ any imperfections in electrode surface quality or alignment may cause arcing at lower voltages. We aim for a more conservative field of 7 kV/mm between electrodes, which requires operating the decelerator with sinusoidal voltages that have an amplitude of 10 kV. This gives a maximum on-axis electric field of 3.2 kV/mm and a Stark potential well depth of 0.57 K for deuterated ammonia molecules (mass ~ 20 amu, dipole moment ~ 1.5 D).

While there are methods to decelerate with lower peak voltages, such as starting with a lower velocity beam,^{18,21} using multiple types of deceleration,^{6,7,14,22} or using a longer decelerator,¹⁹ our goal is to decelerate a supersonic beam seeded in krypton using only TWSD in a 1.25 m long decelerator. The choice of a krypton expansion in a 1.25 m long decelerator is the result of a compromise between competing factors. Heavier seed gasses create slower molecular beams but also have an increased rate of clustering, which reduces signals.¹³ We find krypton to be the heaviest seed gas that also gives adequate signals. The low initial velocity of a krypton expansion allows for a shorter decelerator, which reduces the cost and time required to construct and align a longer decelerator.¹⁹

In addition to the voltage requirements, the amplifier must be able to supply the current required to charge the capacitive load of the decelerator. The effective capacitive load of our decelerator is calculated to be 225 pF,²³ which does not include the capacitance of any cabling between the amplifier and decelerator. Unshielded cables could be used, which would add no additional capacitance. We use coaxial cables and estimate that our cables add around 40 pF/ft. Even if the amplifiers are mounted close to the vacuum electrical feedthroughs, ~ 2 ft of cable is still required. The additional cabling adds significant capacitance to the load, which the amplifiers must drive. Using the effective capacitance of the decelerator, the maximum frequency of 30 kHz, and the maximum

± 10 kV output, we determine that the amplifiers must be able to source and sink a peak current of ~ 0.5 A. In order to allow for added capacitance due to cabling and flexibility in the output waveform, the design goal for the amplifiers was set at 1.5 A.

Finally, the design of the amplifier must be able to dissipate the heat generated by the high voltages and currents present. The electronics of the amplifiers do not prevent the amplifiers from being run continuously; however, this would create an unmanageable thermal load and require the dissipation of several kilowatts. Instead, the experiment runs at 10 Hz and requires the amplifier to be on for ~ 6 ms in order to bring the molecules to rest. This means that an amplifier must be able to dissipate ~ 200 W when running in a pulsed mode.

Implementation of TWSD has been limited by these challenging bandwidth, voltage, and current requirements. While several commercial amplifiers are able to meet some of these criteria, none meet all. The closest is the Trek 5/80 amplifier, which has been used in several TWSD experiments.^{14,19,21} It has a bandwidth of greater than 60 kHz down to DC and a maximum output voltage of ± 5 kV at peak currents of 500 mA.²⁴ The custom amplifier presented here is capable of ± 10 kV peak amplitudes and peak pulsed currents of 1.5 A and has a bandwidth of 30 kHz down to DC, which means it can produce the waveforms needed for TWSD in an apparatus that is 1.25 m in length.

II. DESIGN OF THE HIGH-VOLTAGE AMPLIFIER

The design of the high-voltage amplifier is based on an optically coupled, all n-channel push-pull amplifier, shown

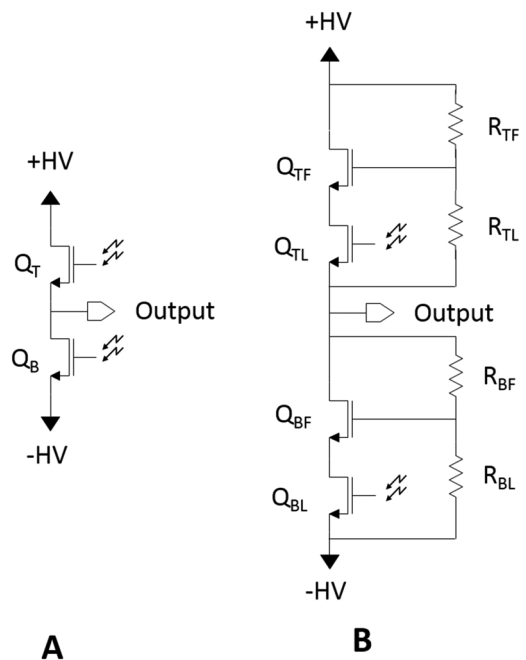


FIG. 1. (a) An optically coupled, all n-channel push-pull amplifier. The \pm HV rails and output voltage are limited to half the voltage rating of a single FET (Q_T or Q_B). (b) With multiple FETs connected in series between the HV rails and the output, a higher maximum output voltage can be achieved. The resistor network divides the voltage between the source and the output such that the voltage is shared equally across each FET.

conceptually in Fig. 1(a). A FET based push-pull design was chosen as the simplest method to stack FETs in series to handle the high voltage. While transformer amplifiers have been used,¹¹ they lack the bandwidth required for decelerating to rest for trapping. In the push-pull design, current is sourced to the load when the top FET (Q_T) is conducting and the bottom FET (Q_B) is non-conducting. When the opposite is true, current is sunk out of the load. Since the FETs operate out of phase, a separate optical control signal is required to drive each FET. A push-pull amplifier could also be made with both n-channel and p-channel transistors. Here, we use all n-channel devices to take advantage of their superior voltage and power handling specifications.

To determine how many n-channel transistors are required for a given application, one should consider the maximum voltage drop across a FET. If the output voltage swings the full range from the positive to negative rail voltages (i.e., +HV to -HV), a single FET, Q_T or Q_B , will experience a voltage drop of $2|HV|$. If this is greater than what one individual FET can handle, multiple FETs in series will be required. In our design, as multiple FETs are added in series, one FET will be driven by an external signal, while all other FETs follow in response to the leading FET. A signal-driven FET is referred to as a leader and the following FETs are referred to as the followers (In some contexts, these are referred to as master and slave circuits, but here we use the terminology leader and follower). Figure 1(b) illustrates how this is accomplished. It has a similar configuration to Fig. 1(a), with Q_{TL} and Q_{BL} being the leader FETs driven by an external signal, but now with additional follower FETs Q_{TF} and Q_{BF} . The resistor chain on the right (R_{TF} , R_{TL} , R_{BF} , and R_{BL}) is a passive voltage divider, which allows each FET that is part of the same bank to share the voltage equally. When all FETs are off, the majority of the current flows down the resistor chain, and only a small leakage current flows down the chain of FETs. If all resistors have the same value, the voltage drop across each FET is the same. If Q_{TL} begins to conduct due to a control signal applied to the gate, the voltage across it and R_{TL} will drop. This reduces the current through R_{TL} . With the current through R_{TL} less than the current through R_{TF} , the net current will flow into the gate of Q_{TF} and turn it on. Thus, whenever the voltage across Q_{TL} does not match that across Q_{TF} , a current will flow into or out of the gate of Q_{TF} to maintain the voltage sharing between Q_{TL} and Q_{TF} constituting passive, local feedback in each bank. This same process occurs if additional follower FETs are added in series.

All of the FETs in series, as well as all other components between the +HV (-HV) rail and the output, are collectively referred to as the top (bottom) bank. Each bank can be thought of as a three terminal device, with an optically controlled gate, a drain end, and source end. Within a single bank, each high-voltage FET and its associated sub-circuits are referred to as one stage of the amplifier. Additional follower stages can be added to each bank at the drain end, and each follower circuit will follow the leader as outlined above.

While the push-pull design in Fig. 1(b) contains the basic block structure of the amplifier, the full design of the amplifier is much more complex. As more followers are connected, additional care must be taken to ensure that all stages share

the voltage equally, so that the FETs are not damaged by being over-voltaged. Failure to do this can lead to catastrophic destruction of the amplifier. The full circuits for both the leader and follower, and their relevant sub-circuits, are discussed below separately before a discussion of the amplifier control, feedback, and physical design.

A. Leader stage

The leader stage acts as the control center of each bank. Figure 2 shows the full leader circuit, which consists of four primary blocks labeled with letters: a high-voltage cascode (A), global feedback driving circuitry (B), a local power supply (C), a local feedback network (D), as well as protection diodes and a few other components for biasing and current limiting. While many of the components in the leader stage float high above earth ground and experience only a few volts of potential difference, the HV MOSFET (Q_1) of the HV cascode, the local feedback network (R_6 , R_7 , C_2 , and C_3), the protection diodes (D_2), and the biasing network (R_{22} , C_9) all experience the voltage drop across the entire leader stage. These component must all be rated to withstand at least 4 kV, which is the maximum voltage rating of the MOSFETs.

A high-voltage BJT-MOSFET cascode, consisting of Q_1 and Q_2 , is used instead of a single FET [Q_T from Fig. 1(b)] to handle the primary voltage drop in the leader stage. In the cascode configuration, the BJT driven by an external signal, Q_2 , will swing only a diode drop between being fully open to fully closed. This is achieved by placing a common-gate, high-voltage stage, Q_1 (IXTF1400 from IXYS), between the signal-driven transistor (Q_2) and the load. Overall, the cascode configuration reduces the Miller effect and increases the speed and stability of the high-voltage handling FET.²⁵ Additionally, the cascode reduces the amount of current required to turn on Q_2 and therefore the amount of current pulled from the voltage division chain.

The global feedback driving circuitry for the main cascode is contained in Fig. 2 Box B (Q_{10} , Q_{11} , Q_{12} , R_{15} , and R_{16}). Q_{11} is a phototransistor and the end of an optoisolator. This separates the low, ≤ 1 V, control signal from the high-voltage potentials on the amplifier and any associated high-voltage noise. Q_{10} is a diode-connected transistor, which, together with R_{15} , acts as a low-current pulldown for the base of Q_{11} , enhancing the turn-off speed of the phototransistor. Additionally, Q_{10} and R_{15} provide emitter degeneration feedback, which helps to stabilize the dc bias against changes in temperature. Together, Q_{10} - Q_{12} form an inverted cascode, which sources current to the base of Q_2 . The inverted cascode prevents large voltage swings at the base of Q_{11} , reducing the amount of current needed to charge and discharge the Miller capacitance, further increasing the speed of the phototransistor. Q_2 then adjusts the voltage on its collector to set the voltage drop between the gate and the source of Q_1 such that Q_1 and Q_2 conduct the same current. When no drive current is present, R_{19} pulls down on the base of Q_2 and closes the stage. At a peak output current of 1.5 A, Q_2 needs 6 mA of gate current, which is provided by the feedback driving circuitry.

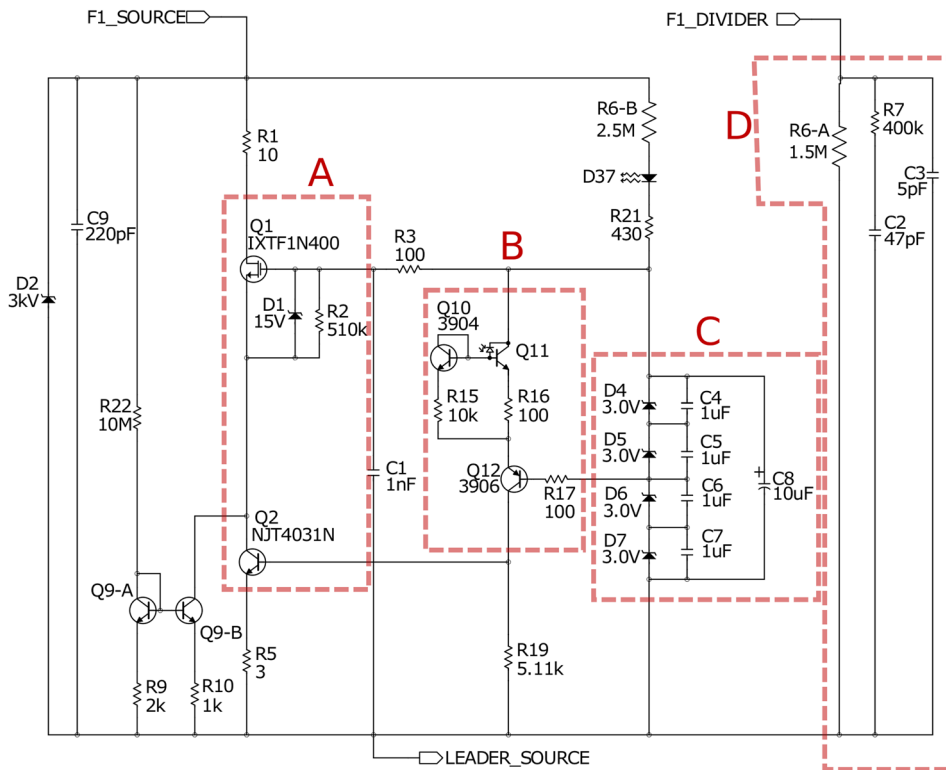


FIG. 2. A leader stage of the high-voltage amplifier. Portions of the circuit are boxed to help identify sub-circuits, these include the (A) cascode, (B) global feedback driving circuitry, (C) local power supply, and (D) local feedback. While some components are high-voltage components, others are standard low voltage components that float up to high potentials but do not experience a large voltage difference. Components that are high-voltage components are indicated in the text.

In order to source and sink the current required to charge the Miller capacitance of Q1, a low-impedance voltage source is required. Box C in Fig. 2 (D4-7 and C4-8) contains a 12 V local voltage supply, which is charged through the high-voltage rail via R6b. For the range of currents drawn by Q1, capacitor backed Zener diodes are an effective low-impedance source and store enough charge to adequately charge and discharge the gate capacitor of Q1. While running the amplifier at full voltage at 30 kHz, the gate capacitance of Q1 draws up to 10 mA and the local power supply will sag only a few millivolts from 12 V. D37 serves as an indicator when troubleshooting to make sure the stage powers up correctly and the local supply stays charged.

The local feedback and passive voltage sharing chain is shown in Fig. 2, box D (C2, C3, R6b, and R7). It serves as a replacement for R_{TL} in Fig. 1. The additional capacitor and resistor-capacitor in parallel help to prevent run away oscillations, while still maintaining fast feedback to the gates of the follower stages. As seen in Fig. 1(b), this portion of the circuit is relevant only when follower stages are included.

A chain of protection diodes, D2, consisting of seven 429 V transient voltage suppression diodes in series, limits the absolute maximum voltage across the leader stage to 3 kV and protects the stage from being reversed biased. The high-voltage MOSFET, Q1 has a maximum V_{DSS} of 4 kV. The protection diodes guard against any poor voltage sharing between stages, transient voltage spikes, or effects of human error during construction and testing.

The final, unboxed components provide current limiting and biasing. R5 limits the instantaneous current that flows down the cascode. Its resistance is chosen so that Q12 will go into saturation when the emitter current of Q2 is greater

than 1.5 A, the maximum current for this design. Biasing of the leader circuit is important to maintain linearity and bandwidth of the optoisolator and stability of the cascode. Biasing Q1 so that it conducts a small quiescent current increases the turn-on stability, linearity, and speed of the BJT. This quiescent current is created via Q9, which acts as an imbalanced current mirror. As long as there is a voltage drop across the stage, current flows through Q9a via R22. The other half of the mirror, Q9b, ensures that Q1 is slightly biased on with a low quiescent current. With rail voltages of ± 15 kV, the quiescent current is 300 μ A. In addition to the quiescent current, a standing current is applied just before, during, and just after the desired output signal. This is applied through the control circuitry and biases on all stages and the optoisolators to help to reduce non-linear amplifier behavior, such as crossover distortion. Typically, the standing current is set at 10 mA and is enabled 1 ms before to 1 ms after the desired waveform. Larger standing currents would further reduce non-linearities but would require a significant amount of power dissipation.

B. Follower stages

The follower circuit, shown in Fig. 3, is very similar to that of the leader circuit, and we will discuss the differences, rather than the similarities. The primary objective of the follower is to mimic the behavior of the leader stage as fast as possible. The communication between the leader and the follower stages occurs through the local feedback voltage divider network. The voltage drop across each stages is determined by the current flowing through the voltage divider. Therefore, any current flowing out of the voltage divider will negatively affect

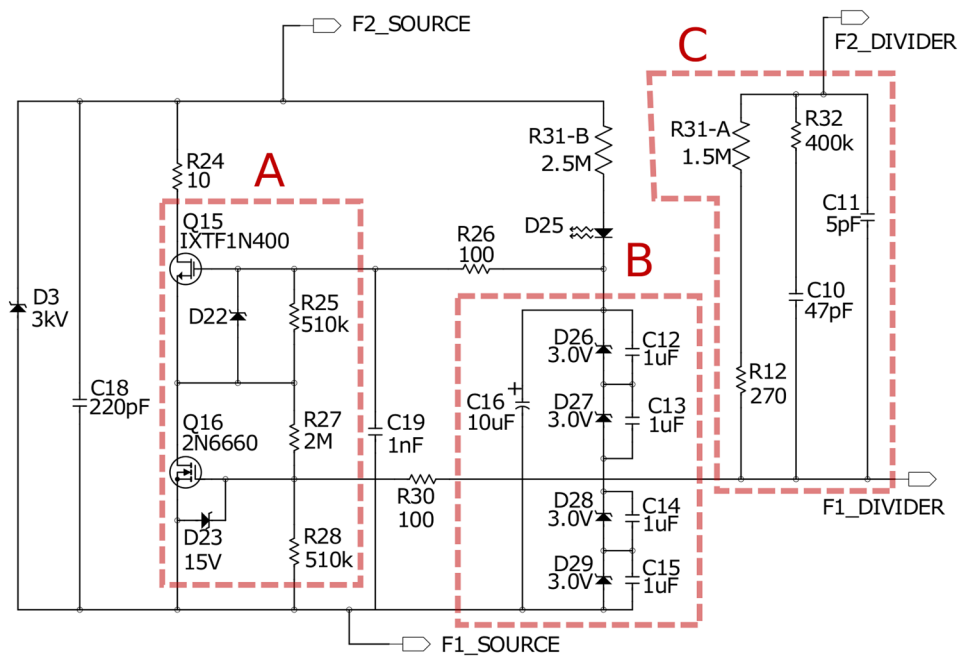


FIG. 3. A follower stage of the high-voltage amplifier. Portions of the circuit are boxed to help identify sub-circuits, these include the (A) cascode, (B) local power supply, and (C) local feedback.

the accuracy of the local feedback. However, in order for the voltage divider to act as passive feedback, it must source the current necessary to control the signal driven transistor in the high-voltage cascode, as shown in Fig. 1. In order to reduce the current needed to turn on the signal-driven transistor, the cascode circuit on the follower (Q15-16) is a FET-FET cascode. The same IXTF1N400 high-voltage MOSFET (Q15) is used, while the lower voltage, signal-driven MOSFET is a 2N6660 (Q16). Q16 then requires negligible drive current from the local feedback network. The pulldown resistor has also been changed from 5.11 k Ω to 510 k Ω , which greatly reduces the current drawn from the local feedback network to keep the gate of Q16 charged. Additionally, the FET that is driven by the external signal is faster than the BJT. For the leader stage, the linearity of the signal-driven BJT transistor is important because any nonlinearities on the leader are corrected only through the relatively slow global feedback. For the follower stages, any nonlinearities are corrected through the fast, local feedback, so the speed of the signal-driven transistor is more important than the linearity. While global control, like the optoisolator in the leader, could also be employed on the follower circuit, only local control, via the resistor-capacitor divider chain, is used. This reduces the complexity of the follower stage and of the global feedback network overall. Therefore, there is no control signal cascode on the follower, although there is still a local power supply to drive the high-voltage FET of the cascode. Additionally, there is no biasing circuitry on the follower stages as they will follow any biasing on the leader stage.

C. Feedback and control

The amplifier contains both local feedback between the leader and follower circuits of each bank via the resistor-capacitor chain and global feedback between the external control signals and the amplifier. The amplifier is operated

via a control board that uses control voltages from an arbitrary waveform generator to generate the required amplifier control signals using a proportional integral differential (PID) loop for global feedback. Additionally, the control board monitors the output voltage, output current, and various other values such as the temperature of the amplifier. Ultimately, the global feedback, local feedback, and rail voltages determine the fidelity of the amplified output voltage.

In order for the feedback to function properly, the stages must be biased correctly, which is achieved by having the amplifier connected to a power supply that can keep rail voltages adequately above the desired output voltage. As long as the stages share the voltage equally, one bank with ten stages (one leader and nine followers) can support up to a 30 kV potential difference across it. Ideally, the output will not swing the full range between the rails, but if it does, one bank will see the full potential between the two rails. This means the maximum rail voltage should be half of what the transistors in series on one bank can handle. In this design, since one bank is designed to have a maximum potential difference of 30 kV, a maximum voltage on the rails is ± 15 kV.

The power supplies for the rail voltages must be backed by capacitors so that enough current can be supplied when the amplifiers are active. We use a Spellman SL150 and a 1 μ F, 20 kV capacitor for each rail. The supplies cannot charge the backing capacitors as quickly as they are drained by the amplifiers, and as a result, the rail voltages sag a small amount during the time the output is enabled. The smallest possible capacity backing capacitor should be used in order to avoid unnecessary energy storage. In the event of an amplifier failure, all the energy may be discharged through some portion of the amplifier. The more energy that is stored, the more dangerous and destructive a discharge will be.

Under normal operation, the rails are kept a few kilovolts above the desired maximum output voltage. The amplifier operates best with at least 100 V across each stage at all times.

Thus, with 10 stages on each bank, the rail voltages should be at least 1 kV above the maximum desired output voltage. In practice, especially when running in the 20-30 kHz range, having the rails 2 kV or more above the maximum desired output voltage is preferable, due to the increased current demands that will increase the voltage sag on the backing capacitors. If the rails sag below the desired output voltage, the output amplitude will be diminished and will clip until the rail voltage can recover.

A second reason to keep the rail voltages several kilovolts above the output voltage is to help produce high fidelity waveforms at higher frequencies. As more followers are added to the circuit, delays in the local feedback chain increase and affect the bandwidth of the local feedback, as well as the voltage sharing between stages. For example, a delay in the local feedback will cause a time delay between the leader and the followers. At high frequencies, this time delay may be a significant fraction of a period, affecting the final output of the amplifier. This causes the control signal to turn on/off the leader more than it would in the ideal case in order to make up the difference between the desired and actual voltage output. When the leader is driven fully open, it has only a very small voltage drop across it, and then must wait for the follower stages to catch up before the local feedback circuit can function again. While this does not lead to instabilities in the amplifier, it does lead to distortions in the output waveform.

To provide the error signal for the global feedback, a custom 20 kV 1500:1 high-voltage divider acts as a high-voltage probe to monitor the amplifier output. The high-voltage divider is designed to have fast rise and fall times of a few hundred nanoseconds and a relatively flat frequency response between DC and 1 MHz. This feedback is enabled only when the standing current is running and the optoisolators are biased on. When not enabled, the local feedback provided by the bias chain is enough to keep the amplifier output near ground. On the control board the error signal is half-wave-rectified, summed with the DC offset that sets the standing current, and sent to each bank's optoisolator light-emitting diode (LED).

Ideally, the amplifier should have constant gain across the entire frequency range. This is mostly accomplished via careful tuning of the global feedback loop. However, if this is not possible to do to an acceptable level with a particular amplifier, a linear scaling function can be applied in the control software, which calculates the input voltage waveform in order to force the amplifier to have a constant amplitude across the frequency range. This allows a final tuning so that each amplifier will have the same output voltage regardless of variation in components and assembly.

The control circuitry also contains circuits for monitoring the output voltage and current of each bank, the cooling fan speed, and the proximity of the output voltage to the rail. If either of the last two monitors fall out of their normal operating range, the amplifier is disabled. When running multiple amplifiers, as is required in TWSD, each individual control board communicates with a master interlock. The master interlock monitors the pressure and flow of the cooling water to all amplifiers, error state of the high-voltage power supplies, and

error state of all running amplifiers, all in hardware. If the master interlock detects an error on any one of these channels, it will shut down all amplifiers.

D. Physical construction

The full amplifier consists of two banks each with one leader and nine follower circuits. Schematically, the source end of the first follower circuit connects to the top, drain end of the leader circuit at the points labeled *F1_Source* and *F1_Divider* (Fig. 3). When connecting multiple followers, each subsequent follower, $n + 1$, is connected to follower n by incrementing the numbers at the *Source* and *Divider* points by one. Because only n -channel high-voltage MOSFETs are used, the source of the follower stage connects to the drain of the leader. Since the leader must always be at the lowest absolute voltage, it must be the source end of each bank. This results in the top bank leader being referenced to the output voltage [just like Q_T in Fig. 1(a)] and the bottom bank leader being referenced to the negative high-voltage rail. The *Source* and *Divider* points of the last (furthest away from the leader) follower are electrically connected to the positive high-voltage rail (output) on the top (bottom) bank. This configuration leads to both banks being identical in construction, but a small asymmetry in operating characteristics, as current is sourced to the load by the leader of the top bank and is drained from the ninth follower of the bottom bank.

Considerations must be taken into account for the safety of the user and the amplifier including circuit layout, cleanliness, insulation, and cooling. The two banks are carefully constructed in order to minimize possible damage from capacitive coupling, corona discharge, and arcing, which all lead to degradation or destruction of the circuit. Sharp points and ragged solder joints on the circuit board lead to corona discharge, which can corrode components. In order to avoid this, the solder joints for all through-hole components are rounded off to be smooth hemispheres. The layout of the printed circuit board (PCB) uses large ground planes that are isolated from the signal traces to prevent capacitive coupling. Additionally, the components for the global feedback on the leader stage (Q10-12) are located on the underside of the PCB board to reduce crosstalk with the HV signal. Finally, the local source planes for each stage are separated by 8 mm to prevent arcing between stages.

Care must also be taken to keep the boards clean and free of dust and grease. All handling of the amplifier banks was performed while wearing gloves to prevent contamination with oils. Solder with water soluble flux was used to aid in cleaning. Once populated, the circuit boards were lightly scrubbed and placed in an ultrasonic bath to remove any flux, oils, or dust.

Even with these precautions, the amplifier can exhibit corona discharges and voltage instabilities. These can be suppressed by insulating the high-voltage circuit boards. Each bank is potted in an insulating, and thermally conductive, room-temperature-vulcanizing silicone, Insulcast RTVS 3-95-1. This material is chosen for its high thermal conductivity and ease of use. The silicone seals around electronic components when it is applied, but does not adhere strongly. This allows

for repairs to the board with no damage from removing the potting material. Other portions of the setup that sit at the output potential, including the output cable and feedback probe, are also potted.

The two potted amplifier banks are installed in a custom high-voltage, shielded box with active cooling (Fig. 4). The box is constructed in two layers: an internal, insulating layer made of polycarbonate, and an external, grounded layer constructed from aluminum. Both layers of the box entirely enclose the amplifier assembly with small holes for signal pass-throughs and ventilation. The fully assembled box measures 3 in. tall, 17.75 in. wide, and 8 in. deep.

The walls of the box where the high-voltage MOSFETs are mounted must simultaneously provide electrical isolation and cooling to the amplifier banks. The IXTF1N400 MOSFETs handle the majority of the voltage drop across each stage and thus the majority of the power dissipation. If the amplifier runs from rail to rail at ± 15 kV and at 30 kHz, the high-voltage MOSFETs will each dissipate 340 W, which is nearly impossible to remove via water cooling. By running the amplifiers in a pulsed mode with only a few percent duty-cycle, as they would be during TWSD, the heat generated drops to roughly 10 W per MOSFET. While this thermal load is manageable, water cooling of the MOSFETs is required. Typically, the MOSFETs can be cooled directly through the isolated back tab, which is normally held at ground. However, because each stage floats many kilovolts above earth ground, the MOSFET back tab cannot be grounded. Instead, the back tab of each MOSFET is electrically connected to its source. Thus, cooling the MOSFETs requires a method that is thermally conductive, but electrically insulating, so that the source plane of each MOSFET remains isolated from all the other MOSFETs. To accomplish this, the sides of the box have boron nitride sheets set into the polycarbonate and water cooling lines are run through the grounded, metal sides. Boron nitride is a ceramic with good thermal conductivity and is also electrically insulating. The boron nitride is sandwiched between the MOSFET and the water-cooled aluminum wall, thus maintaining insulation between the large potential differences of the MOSFETs and the exterior grounded box. The boron nitride pieces are glued in place using MG Chemical's 4226 *Super Corona Dope*. The interior wall and the outer aluminum wall are screwed together and thermal paste is applied between them on the boron nitride portions in order to facilitate cooling. The IXTF1N400 MOSFETs are mounted such that their back tab is in direct contact with the boron nitride.

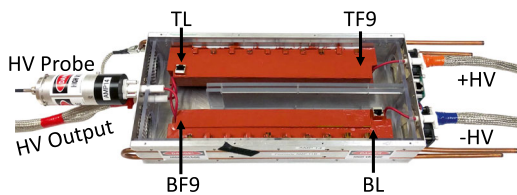


FIG. 4. A photograph of the amplifier with the top lids removed. The cables between the rail voltage supplies and the amplifier are on the right and the output, which can connect to the decelerator, and the probe for global feedback are on the left. For the top (bottom) bank, the leader TL (BL) and last follower TF9 (BF9) are labeled.

III. AMPLIFIER PERFORMANCE

A. Testing setup

The amplifier is tested on the bench using a high-voltage capacitor, C_l , connected as a test load to substitute for the Stark decelerator. A schematic diagram of the testing setup is shown in Fig. 5. The amplifier has been tested with loads that vary from 125 pF to 500 pF in order to test different current requirements without changing the output voltage. A $10\ \Omega$ sense resistor is placed between the load capacitor and ground in order to monitor the load current. A Tektronic P6015A 1000X probe is used to measure the output voltage of the amplifier. A 1000:1 voltage divider is a part of the global feedback and PID control system.

The amplifier is tested with single frequency and chirped sine-wave pulses 1-5 ms long as well as with low frequency square-wave pulses. The length of the pulses is limited by the size of the backing capacitors. With larger capacitors or a power supply capable of sourcing 1.5 A, the length of the pulses would be limited only by the cooling of the amplifier. Single-frequency pulses are used to characterize gain, phase-slip, and distortion across the bandwidth of the amplifier. Square-wave pulses are used to characterize rise and fall times, and time delays. Finally, while there are many types of sinusoidal pulses that can be used to decelerate molecules, linearly chirped sine-wave pulses are shown because they will be the signals used most typically with traveling-wave Stark decelerators.

B. General specifications

The general specifications for the amplifier are listed in Table I. The amplifier is designed for a peak output voltage of ± 12 kV but has only been tested in this work to ± 10 kV in order to maintain linearity and stability. Thus, the gain is designed to be 12 000 with a maximum input of ± 1 V. The design goals for the amplifier emphasize bandwidth, output voltage, and current. The bandwidth of an amplifier can be classified in a number of ways, with the most common being

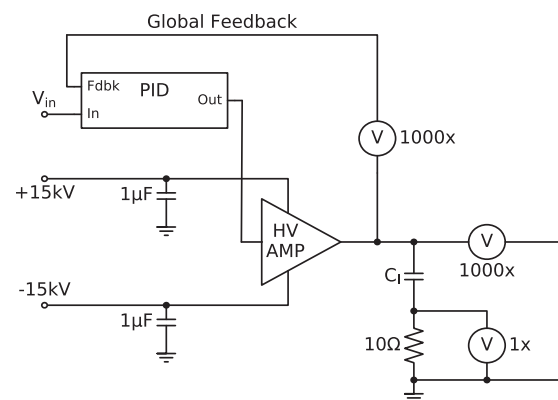


FIG. 5. The test setup for measuring the output voltage and current. The 250 pF capacitor acts as the output load. There is a 1000X probe used to measure the output voltage of the amplifier and another to divide the voltage for the global feedback loop. The $10\ \Omega$ resistor is a current sense resistor, and the 1X probe is used to monitor the output current of the amplifier. All components other than the $10\ \Omega$ sense resistor must be rated for high-voltage.

TABLE I. Technical parameters of the amplifier.

Parameter	Value
Max input voltage range	± 1 V
Output voltage range	± 10 kV
Gain	12 000
Load	Up to 500 pF
Peak current	± 1.5 A
Bandwidth	$>30^a$ or 23^b kHz
Noise	$300 \mu\text{V}/\sqrt{\text{Hz}}$
Harmonic distortion ^c	1.4%
Supply voltage	± 15 kV

^aCalculated from gain fall-off.

^bCalculated from THD measurements. Limit 5% THD on 250 pF load.

^cMeasured at 10 kHz with a 500 pF load.

the -3 dB point of the amplifier's gain curve. The gain curve for our amplifier, under three different load conditions, is shown in Fig. 6. The gain curve shows relatively little deviation from the target gain of 81.6 dB, especially for the 250 pF load, indicating that the amplifier bandwidth extends beyond the target of 30 kHz. The amplifier was not tested above 30 kHz at 20 kV_{pp} because the local feedback may not be fast enough to ensure even voltage distribution between the stages, and a single stage may be overvoltaged. However, tests at 10 kV_{pp} show the -3 dB point to be beyond 40 kHz for all load capacitances tested.

While the gain curve indicates a bandwidth greater than 30 kHz, the quality of the amplifier output begins to deteriorate beyond 18 kHz. One measure of output signal fidelity for high-voltage amplifiers is Total Harmonic Distortion (THD).²⁶ THD compares the amplitude of the Fourier component of the peak frequency against the amplitude of all higher order harmonics and indicates the distortion from an ideal, single-frequency wave. If V_n labels the n th harmonic amplitude, then THD is defined as

$$\text{THD} = \frac{1}{V_1} \sqrt{\sum_{n=2}^{\infty} V_n^2}. \quad (2)$$

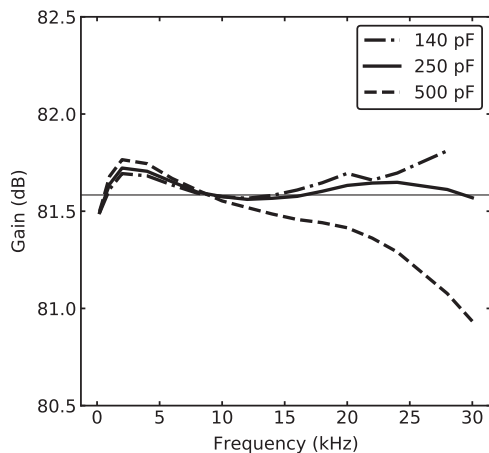


FIG. 6. Measured gain of the amplifier. The solid horizontal line is located at 81.6 dB, which is the target gain of the amplifier. The gain was measured using an input single-frequency sine wave with a peak-to-peak amplitude of 1666 mV_{pp}.

Distortion of the sine wave will appear “smooth” if the amount of power in the higher harmonics decreases with increasing harmonic number. An example of two output waves with their Fourier transforms is shown in Fig. 7. Although the 30 kHz waveform shows a significant THD of 11%, the distortions appear smooth due to the decreasing power of the higher order harmonics. An analysis of the THD across the frequency range shows that the THD stays below 2% for frequencies below 18 kHz. The THD then rises sharply for frequencies above 18 kHz to a final value of 11% at 30 kHz.

For applications where amplitude is a primary concern, the bandwidth is greater than 30 kHz. For applications where waveform fidelity is of concern, a bandwidth of 18-20 kHz is more relevant. The relatively large amplitudes of the even-ordered harmonics indicate an asymmetric distortion between the positive and negative sides of the wave, which is evident in the time-domain waveform. This is due to the asymmetric nature of the all n -channel-MOSFET amplifier construction noted earlier.

The output voltage of the amplifier was tested at ± 10 kV. The gain curve shown in Fig. 6 was taken with a constant amplitude input sine wave of 1666 mV_{pp} and shows a near-constant gain of 81.6 dB, giving a constant output of 20 kV_{pp} across all frequencies. As tested, the amplifier reached a peak current of 860 mA, while driving the 500 pF load at 30 kHz. This is significantly above the 500 mA needed to charge the 250 pF load of our Stark decelerator.

Additional tests were performed with a square wave to measure rise and fall times and time delays. The results of these tests are summarized in Table II. The values for rise and fall times highlight the asymmetry introduced through the

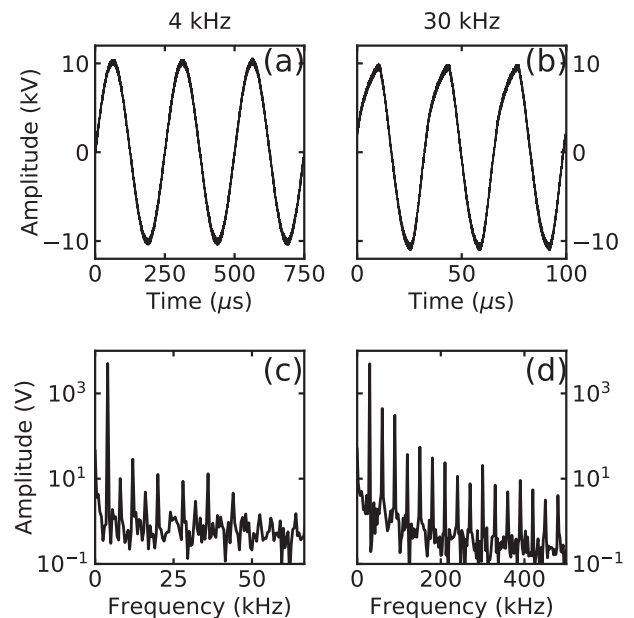


FIG. 7. Measured output sine waves and their respective Fourier transforms for 4 kHz [(a) and (c)] and 30 kHz [(b) and (d)] input sine waves on the 250 pF load capacitor with ± 13 kV rails. The x-axes are scaled such that there are the same number of periods (3) and harmonics (15) shown for each of the frequencies. (a) The time domain and (c) frequency domain response for a 4 kHz input sine wave have a calculated THD of 0.7%. (b) and (d) are the same for a 30 kHz input sine wave, with a calculated THD of 11.0%.

TABLE II. Small-signal amplifier parameters. Rise and fall times, t_r and t_f , and delay d were taken with a 1 kHz square wave with an output of V on a load capacitance of C_l . The rails were held fixed at ± 11 kV.

V (kV _{pp})	C_l (pF)	t_r (μ s)	t_f (μ s)	d (μ s)	S^a (V/ μ s)
10	125	3.9	3.4	2.8	2590
12	125	4.8	3.4	2.8	2530
10	250	4.2	4.4	3.2	2320
12	250	5.3	4.4	3.2	2260
10	500	4.9	6.2	3.9	1630
12	500	5.6	6.2	3.9	1920

^aSlew rate is calculated from peak amplitude and the larger of t_r or t_f .

all n-channel-MOSFET construction of the amplifier banks. While the fall time, controlled by the bottom bank sinking current from the load, is dependent only on the capacitance of the load, the rise time is dependent on both the capacitance and the output voltage. This indicates that the output current that the top bank can source is dependent on how far the output voltage is from the rail voltage.

The asymmetries presented here are a product of the single-leader, all n-channel design. Introducing an optically coupled sub-leader in place of follower number 5 would allow more feedback throughout the amplifier bank but would also complicate the driving and feedback tuning of the amplifier. A design that utilized p-channel FETs in the bottom bank may also produce a more symmetric output. However, the lower voltage handling capability of p-channel FETs would require many more stages. This would increase the sharing error between stages and possibly introduce more asymmetries.

C. Voltage sharing

Voltage sharing between the stages of the amplifier via the local feedback is critical to the stability of the amplifier in order to assure that no single stage is over-voltaged under any conceivable operating conditions. In order to assess the quality of voltage sharing between stages of one bank, the voltage across each stage is measured by separately probing the voltage at the source end and then the drain end of each stage and then subtracting the signals during post-processing. The source and drain ends of the stage need to be measured separately, or cross talk between the measurement probes' leads can inject current into the stage and drastically alter the stage's functionality.

The largest voltage difference occurs between the stage that is closest to the rails and the stage that is closest to the output. For the bottom bank, these are the leader and ninth follower stages, respectively, and vice versa for the top bank. The behavior of the two banks is similar, and the following discussion refers only to the bottom bank. The ratio between the voltage across the ninth follower stage to the voltage across the leader stage is shown in Fig. 8. Data were taken at 4, 20, and 30 kHz, and at amplitudes from 2 kV_{pp} to 8 kV_{pp}. Higher amplitudes were not tested because measuring voltages across stages requires probing inside the amplifier while it is running, which requires the potting material to be removed from the circuitry. This, in turn, decreases the stability of the

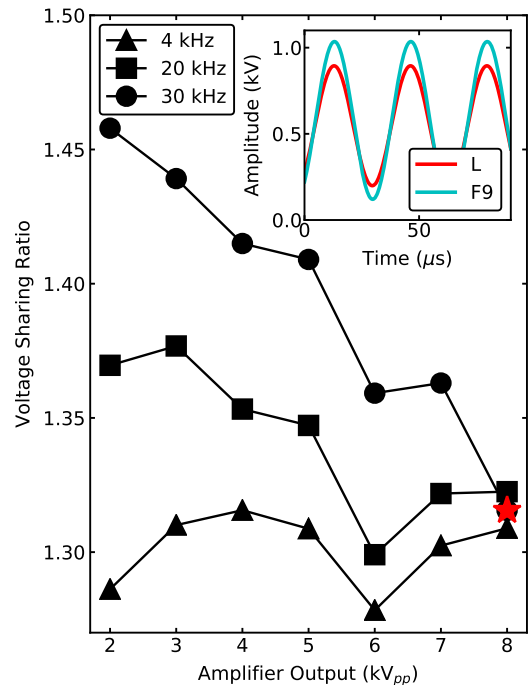


FIG. 8. Ratio of voltage dropped between the final follower stage (F9) and the leader stage (L) on the bottom bank for three different frequencies. The voltage sharing for high frequencies is poor at low voltages but stabilizes as the output voltage increases. All data were taken with rail voltages of ± 6 kV. The inset shows the sine fit of the waveforms for the voltage across the leader and final follower at 30 kHz and at 8 kV_{pp}. The point at which these data were taken is highlighted on the main plot with the red star.

amplifier and increases the likelihood of corona effects at high voltage.

Figure 8 shows that while higher frequency signals cause the amplifier to share poorly at low voltages, increasing the output voltage increases the stability of the local feedback network at high frequencies. The voltage across the final follower stage reached about 1.33 times the voltage across the leader. The inset shows a sine fit of the measured voltage on both stages. While the amplitude difference is clear, there is very little phase shift between the two signals.

The voltage sharing ratio is a measure of how well the voltage is distributed across the entire amplifier bank. If the ratio is too large, the ninth follower stage could experience too large a voltage drop and could become overvoltaged. To determine if the measured sharing ratio of 1.33 is low enough to allow the amplifier to produce a ± 10 kV sine wave with ± 13 kV rail voltages without overvoltageing any stage, we consider the following calculation.

The mean voltage across a stage, \bar{V} , is defined as one tenth of the voltage across an entire bank and is the ideal case for the amplifier. A voltage sharing ratio different from unity indicates that the voltage across the leader and ninth follower are offset from \bar{V} . Measurements of this offset, V_{offset} have shown that it is symmetric about \bar{V} for the leader and the ninth follower. Thus, the voltage drops across the leader and ninth follower are $V_L = \bar{V} - V_{\text{offset}}$ and $V_{F9} = \bar{V} + V_{\text{offset}}$. The sharing ratio is then defined as

$$R = \frac{V_{F9}}{V_L} = \frac{\bar{V} + V_{\text{offset}}}{\bar{V} - V_{\text{offset}}} \quad (3)$$

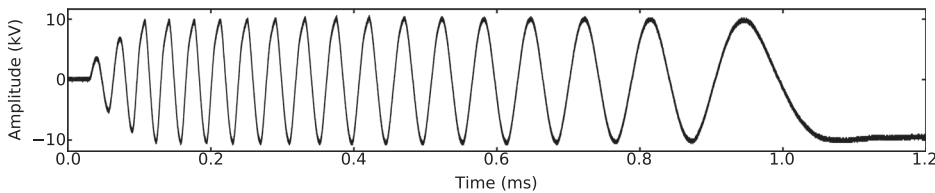


FIG. 9. A linearly chirped voltage waveform from 30 kHz to DC at ± 10 kV. Fewer periods than would be used for TWSD are shown for clarity, and three start-up periods are appended to the front of the wave packet in order to prevent large start-up current spikes.

The maximum value for the voltage across a single stage, V_{\max} , is set by the protection diode chain to be 3 kV. The ninth follower stage is at a higher voltage than the leader stage, and may potentially rise above the diode threshold voltage. This sets a bound on the maximum allowable voltage offset of

$$V_{\text{offset}} < V_{\max} - \bar{V}. \quad (4)$$

Combining Eqs. (3) and (4) gives an upper bound on the acceptable value of the voltage sharing ratio of

$$R < \left(2 \frac{\bar{V}}{V_{\max}} - 1 \right)^{-1}. \quad (5)$$

For the amplifiers to safely produce an ± 10 kV sine wave with rail voltages of ± 13 kV, each bank must be able to withstand a maximum of 23 kV, which sets \bar{V} to 2.3 kV. R must then be less than 1.875 in order for no stage to be overvolted during normal operating conditions. The measured R value of 1.33 is well below this maximum value. Therefore, we do not anticipate this small voltage sharing error to limit the performance of the amplifier.

D. Chirped sine waves

Ultimately, the amplifier will be used for TWSD and must be able to output a chirped sine-wave voltage with uniform output amplitude across the frequency range. A sine wave chirped from 30 kHz to DC at ± 10 kV output voltage is shown in Fig. 9. Here, for clarity, a more aggressive chirp is shown than would typically be used in TWSD. A typical deceleration waveform in our decelerator would have 78 periods in 6 ms. A DC hold is also demonstrated, as this would be required for trapping the molecules. Additionally, a three period start-up sequence, where the amplitude is increased linearly to the operating voltage, is appended to the front of the waveform to prevent the large current spikes necessary to start a sine wave at arbitrary phase from ground. The high frequency part of the waveform shows distortions similar to those in Fig. 7, while the lower frequency part is free of distortions.

IV. CONCLUSION

A new type of Stark deceleration technique called traveling-wave Stark deceleration promises to greatly increase the number and density of cold, slow molecules produced compared to traditional pulsed-pin deceleration. The challenge to implementing TWSD lies in creating high-voltage analog amplifiers with demanding specifications. The bandwidth, voltage, and current requirements needed to bring a supersonic beam seeded in krypton down to rest in 1.25 m are not available in any commercial high-voltage amplifier. The amplifier presented here is capable of output voltages up to

± 10 kV, instantaneous currents up to 1.5 A, and a frequency range from 30 kHz down to DC. The peak voltages of the amplifier will allow the deceleration of small polar molecules such as ND_3 and OH , while the bandwidth will allow for deceleration of a molecular beam with an initial velocity of < 450 m/s down to rest. We have quantitatively measured the voltage sharing error between stages and the total-harmonic distortion. We have demonstrated that the amplifier can operate over the full design frequency range. Additionally, the flexibility of these amplifiers can allow for not only traveling-wave Stark deceleration but also efficient trap loading and manipulation.

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